



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/815,317

04/01/2004

Phil Van Dyke

VP127

7237

20178

7590

07/10/2008

EPSON RESEARCH AND DEVELOPMENT INC
INTELLECTUAL PROPERTY DEPT
2580 ORCHARD PARKWAY, SUITE 225
SAN JOSE, CA 95131

EXAMINER

ABDULSELAM, ABBAS I

ART UNIT

PAPER NUMBER

2629

MAIL DATE

DELIVERY MODE

07/10/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/815,317	Applicant(s) VAN DYKE, PHIL	
	Examiner ABBAS I. ABDULSELAM	Art Unit 2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 July 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6,8-10,15-25,27 and 28 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) 1-6,8-10,15-25,27 and 28 is/are allowed.
- 6) ☒ Claim(s) _____ is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is in response to a communication filed 07/01/2008. Amendments on 07/01/2008 are entered. Claims 1-6, 8-10, 15-25 and 27-28 are pending. Claims 7, 11-14 and 26 are canceled.

Response to Arguments

2. Applicant's arguments filed on 07/01/2008 have been fully considered but they are not persuasive.

On the second through fifth paragraphs of applicant's "REMARKS", applicant summarized the teaching of a reference, Worley III (USPN 6326980), that is used in the rejection.

In response, the examiner notes the summary.

On the fifth paragraph of applicant's "REMARKS", applicant states the following:

"Worely describes arranging the bits of the compound data words in the portions of the compound data words to minimize intensity differences between the respective portions (Worely, column 4, lines 46-49). The bits of the compound data words area arranged to minimize the phase differences between adjacent pixels, note the intensity differences as suggested by the examiner".

The examiner disagrees with the applicant's argument with respect to the examiner's interpretation of the Worley reference. As shown in the art rejection below, and stated by the applicant, Worley teaches arranging the bits of the compound data words in the portions of the compound data words to minimize intensity differences between the respective portions (Worely, column 4, lines 46-49). and the examiner indicates that minimization of intensity differences involves a reduction of power consumption. It is clear that the less the phase differences among adjacent pixels, the less power needed to correct those differences.

Applicant amended independent claims 1, 18 and 20, and argues that the Worley reference does not teach the amended claim limitations.

In response, applicant's arguments are moot in view of the new ground(s) of rejection (see the rejection below).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-6, 8-10, 15-18, 20-25 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Worley III (USPN 6326980) in view of Oki et al. (USPN 5408252).

Regarding claims 1 and 18, Worley, III (USPN 6326980) teaches a digital display system, a data processor(***Fig. 10 (I004, I008, 926, 954), see fig. 10 in which a processing unit I004 controls transfer state machine I008 which outputs via control buses (926, 954)***), electro-optic display(***Fig. 9 (914, 926, 928)***); and a display controller (***Fig. 9 (900)***) for reducing power consumption of an electro-optical image display (***Fig. 9 (900), a display driver circuit 900, col. 4, lines 46-49, bits of a compound data words are arranged in portions of the compound data words to minimize intensity differences between the respective portions, note that minimization of intensity differences inherently involves reduction of power consumption)***), comprising: a

Art Unit: 2629

source of a set of image data words (*Fig. 9 (900, 902)*) corresponding to individual pixels of an image (*Fig. 9 (902), col. 9, lines 28-29, compound data generator 902 receives 8-bit binary-weighted data words*); an output port (*Fig. 9 (914, 924, 926)*) for making available to the electro-optical image display a modified set of image data words corresponding to individual pixels of the electro-optical image display (*Fig. 9 (914), col. 11, lines 15-18, output controller 914 asserts control signals on LCD control bus 926, causing micro-LCD 928 to load the bits asserted on data bus 924 onto the appropriate pixel cells*); and a mode control circuit (*Fig. 9 (908), 924*) adapted to substitute for a selected subset of the set of image data words the image data words from one or more contiguous pixels and to provide the resulting modified set of image data words to the output port to be made available to the electro-optical image display (*Fig. 9 (908), col. 9, lines 43-50, Data planarizer 908 receives the compound data, via compound data bus 936, in 10-bit compound data words, each 10-bits corresponding to a gray scale value to be written to a particular pixel (r) of micro-LCD 928, such that the data planarizer 908 accumulates the 10-bit gray scale data for 32 pixels and reformats the data into 32-bit data words, each 32-bit word containing one bit from each of the group of 32 10-bit compound data words, col. 9, lines 20-24, note that the driver circuit 900 transfers the planarized compound data words, via 32-bit data output bus 924, along with control signals, via LCD control bus 926, to a micro-LCD 928*), and wherein the image data words of the modified set of image data words are made available to the electro-optical display serially, and the contiguous pixels whose image data words are substituted precede the image data words for which they are substituted (*col. 9, lines 20-24, co. 9, lines 43-50, Fig. 9 (908), data planarizer 908 accumulates the 10-bit gray scale data for 32 pixels and reformats the data into 32-bit*

Art Unit: 2629

data words, each 32-bit word containing one bit from each of the group of 32 10-bit compound data words,, note that the driver circuit 900 transfers the planarized compound data words, via 32-bit data output bus 924, along with control signals, via LCD control bus 926, to a micro-LCD, also note that that reformatting the data involves two different sets of data (data prior to reformatting and after reformatting, and data prior to reformatting naturally comes first)).

Regarding claim 20, Worley teaches a method for reducing power consumption of an electro-optical image display (*Fig. 9 (900), a display driver circuit 900, col. 4, lines 46-49, bits of a compound data words are arranged in portions of the compound data words to minimize intensity differences between the respective portions, note that minimization of intensity differences inherently involves reduction of power consumption*), comprising: providing a set of image data words corresponding to individual pixels of an image (*Fig. 9 (900, 902), col. 9, lines 28-29, compound data generator 902 receives 8-bit binary-weighted data words*); substituting for a selected subset of the set of image data words the image data words from one or more contiguous pixels (*Fig. 9 (908), col. 9, lines 43-50, Data planarizer 908 receives the compound data, via compound data bus 936, in 10-bit compound data words, such that the data planarizer 908 accumulates the 10-bit gray scale data for 32 pixels and reformats the data into 32-bit data words, each 32-bit word containing one bit from each of the group of 32 10-bit compound data words*); and making available to the electro-optical image display the modified set of data words resulting from the substituting (*col. 9, lines 43-50, note that each 10-bits corresponding to a gray scale value is to be written to a particular pixel (r) of micro-LCD 928, col. 9, lines 20-24, the driver circuit 900 transfers the planarized compound data words, via 32-bit data output bus 924, along with control signals, via LCD control bus 926, to a*

Art Unit: 2629

micro-LCD 928), and wherein the image data words of the modified set of image data words are made available to the electro-optical display serially, and the contiguous pixels whose image data words are substituted precede the image data words for which they are substituted (col. 9, lines 20-24, co. 9, lines 43-50, Fig. 9 (908), data planarizer 908 accumulates the 19-bit gray scale data for 32 pixels and reformats the data into 32-bit data words, each 32-bit word containing one bit from each of the group of 32 10-bit compound data words,, note that the driver circuit 900 transfers the planarized compound data words, via 32-bit data output bus 924, along with control signals, via LCD control bus 926, to a micro-LCD, also note that that reformatting the data involves two different sets of data (data prior to reformatting and after reformatting, and data prior to reformatting naturally comes first)).

While Worley teaches as shown in Fig. 9, data planarizer 908, which receives the compound data, via compound data bus 936, in 10-bit compound data words, such that the data planarizer 908 accumulates the 10-bit gray scale data for 32 pixels and reformats the data into 32-bit data words, each 32-bit word containing one bit from each of the group of 32 10-bit compound data words (Fig. 9 (908), col. 9, lines 43-50),

Worley does not teach a claim limitation which reads “substituting includes a placing operation on a first image data word and one or more of the image data words that follow the first image data word with the same value as the first image data words, and periodic repeating of the replacing operation with a new first image data words to form a modified set of image data words that are contiguous”.

Oki et al. (USPN 5408252) on the other hand teaches as shown in Fig. 6 a liquid crystal display device including two liquid crystal cells of the pixel pair are connected by the same data bus line 13 (col. 7, lines 56-65, col. 7, lines col. 8, lines, 37-41), Note as shown in fig. 6, that the two adjacent liquid crystal cells of pixels ($LCm, 2n-1, LCm, 2n$) are connected by one same data bus lines $13n$, and the next two adjacent cells of pixels are connected by another same data bus line $13n+1$, similarly, the rest of plurality of adjacent cells of pixel pairs throughout the matrix LCD are connected such that each pair has the corresponding one data bus line (col. 7, lines 56-67). Hence it is clear that data bus driver 214 that is illustrated in Fig. 1 outputs the same data voltage to two adjacent liquid crystal cells of pixels ($LCm, 2n-1, LCm, 2n$) through data bus line $13n$. Similarly, the data bus driver 214 outputs the same data voltage to the next two adjacent liquid crystal cells of pixels through data bus line $13n+1$. Thus, as illustrated in Fig. 6, adjacent cells of pixels that are connected with the same data bus line ($13n$) have the same value, and the next two adjacent cells of pixels that are connected with another same data line $13n+1$ also have the same value but is different from the first value one (since the data line is different). Also note that as illustrated in Fig. 1, the data bus driver 214 is connected and controlled by a controller (218).

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Worley's display driver circuit 900, which includes planarizer 908 as shown in Fig. 9 with Oki's use of same data line 13 for two adjacent liquid crystal cells of pixels as illustrated in Fig. 6, the use of same data line for two adjacent liquid crystal cells of pixels helps improve the display quality as taught by Oki (col. 2, lines 37-40).

Regarding claims 2 and 21, Worley teaches the electro-optical image display is a two-dimensional image display (*Fig. 9 (828), col. 10, lines 7-9; micro-LCD has 786,432 pixels ('1024x768')).*

Regarding claims 3 and 22, Worley teaches the electro-optical image display is a liquid crystal display/the making available is done in a format suitable for a liquid crystal display (*Fig. 9 (828), col. 10, lines 7-9, micro-LCD has 786,432pixels ('1024x768')).*

Regarding claims 4 and 23, Worley teaches the electro-optical image display is a two-dimensional display (*Fig. 9 (828), col. 10, lines 7-9; micro-LCD has 786,432 pixels ('1024x768')).*

Regarding claims 5, 9 and 24, Worley teaches the selected subset of image data words comprises a subset of the image data words having a selected spatial periodicity (*Fig. 20 (2002, 2004, 2006), a field sequential data, col. 19, lines 25-39).*

Regarding claims 6, 8, 10, 25, and 27, Worley teaches the number of contiguous pixels whose image data words are substituted may be selectively determined (*col. 11, lines 51-61, first and second group of pixels).*

Regarding claim 15, Worley teaches the source of image data words comprises a memory and a memory controller (*Fig. 9 (946, 948, 910, 912), control buses (946, 948), frame buffers 910 and 912), and the mode control circuit (Fig. 9 (908, 924), data planarizer (908), data output*

Art Unit: 2629

bus (924)) comprises a display interface circuit (Fig. 9 (924), data output bus (924), note that as shown in Fig. 9, the data output bus (924) is directed toward a micro-LCD (9128)).

Regarding claim 16, Worley teaches an input port (*Fig. 9 (904, 906, 918, 920, 922), input controller 904, a control selector 906, input terminals 918, 920, and 922*) for receiving image information from a data processor for storing an image in the memory (*Fig. 9 (910, 912), col. 9, lines 55-59, note in Fig. 9 in which input terminals 918, 920, and 922 passing signals through input controller 904, which uses the signals to transfer planarized data from data planarizer 908, via 32-bit data bus 930 into frame buffers A 910 and B 912*)).

Regarding claim 17, Worley teaches the input port (*Fig. 9 (904, 918, 920, 922, 906), input controller 904, a control selector 906, input terminals 918, 920, and 922*) comprises a host interface circuit (*Fig. 9 (906), a control selector (906)*) for receiving data and providing that data to the image data memory controller for storage in the memory (*Fig. 9 (910, 912), col. 10, lines 11-13, the transfer of data from data bus 930 into frame buffers 910 and 912 is also controlled by input controller 904 in cooperation with control selector 906*)).

4 Claims 19 and 28, is rejected under 35 U.S.C. 103 (a) as being unpatentable by Worley III (USPN 6326980) in view of Oki et al. (USPN 5408252) further in view of Aoki et al. (USPN 5650844).

Regarding claim 19, Worley (as modified by Oki) does not teach a camera to provide image information to the source of a set of image data words corresponding to individual pixels of the image.

Aoki et al. (USPN 5650844) on the other hand teaches as shown a CCD camera 12 that has a built-in CCD area sensor that measures the contrast of the LCD (Fig. 1 (12) (col. 4, lines 12-18).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine to combine Worley's display driver circuit (900) (as modified by Oki) shown in Fig. 9 with Aoki's CCD camera 12 as shown in Fig. 1, because the use of CCD camera 12 helps function LCD panel image quality inspection as taught by Aoki et al (col. 4, lines 5-6).

Regarding claim 28, Worley teaches the source of image data words comprises a memory and a memory controller (Fig. 9 (900, 902)).

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

Art Unit: 2629

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ABBAS I. ABDULSELAM whose telephone number is (571)272-7685. The examiner can normally be reached on Monday through Friday from 9:00a.m. to 5:30 p.m. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Abbas I Abdulsalam/

Primary Examiner, Art Unit 2629